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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/002,193	10/19/2001	Tuan Van Ngo	TI-31786	2356

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EXAMINER	
KAPADIA, VARSHA A	

ART UNIT	PAPER NUMBER
2651	4

DATE MAILED: 08/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/002,193	NGO ET AL.	
	Examiner	Art Unit	
	Varsha A Kapadia	2651	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-6,11-18,20,22 and 24* is/are rejected.

7)☒ Claim(s) *3,7-10,19,21 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4-6, 13-17, 20, 22 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nayebi et al (6,175,463) in view Pidutti et al (6,166,869).

With regards to claims 1, 13 and 20 Nayebi et al discloses a write driver circuit (see fig.3 and disclosure thereof) having differential input comprising: a write head (L1); an H-switch having first and second transistor (Q2, Q1) having a first node (T1), and a third and forth transistor (Q3,Q4) having a second node (T2) there between. A first boosting circuit coupled to the differential input adapted to pull the first node low and the second node high and vice versa for the second boosting circuit (10a and 10b and disclosure thereof). Nayebi et al also discloses that the boosting circuit is adapted to create larger voltage swing (considered as increase in voltage) and faster slew rate (improving rise time) (see abstract and col.3 lines 27-35).

Nayebi et al fails to specify the elements of the boosting circuit i.e. a transistor set as claimed.

Pidutti et al however discloses a first and a second boosting circuit including a transistor set (see figs. 2 and 4 elements 40, 43-44, 41, 46-47 and disclosure thereof).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the boosting circuit disclosed by Nayebi et al with the above teachings from Pidutti et al in order to specify the details of the circuit components

i.e. transistors since use of transistor in a circuit design is routine engineering and no unexpected results are to occur.

With regards to claims 4 and 24, Pidutti et al discloses that the boosting transistor set includes PMOS transistor (see fig.4 element 44 and 47). Pidutti et al is relied upon for the same reasons.

With regards to claim 22, see Pidutti et al (abstract) Pidutti et al is relied upon for the same reasons as described above in this office action.

With regards to claims 5-6, Pidutti et al discloses that the boosting transistor set includes pair of MOS transistors (see figs. 2 and 4 elements 43-44 and 46-47 and disclosure thereof) but fails to show that both of the transistors are PMOS. However designing a circuit using PMOS or NMOS or combination of both is considered routine engineering design and is considered obvious to one of ordinary skill in the art since no unexpected results are to occur.

Claims 14 -17 are drawn to method of using apparatus claimed in claims 1, 4-6, 13, 20 22 and 24. Therefore method claims 14-17 corresponds to apparatus claims 1, 4-6, 13 20, 22 and 24 and are rejected for the same respective reasons of obviousness as used above.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nayebi et al in view of Pidutti et al as applied to claims 1, 4-6 and 13 above, and further in view of Schuelke et al. (5,757,215).

With regards to claim 2, Nayebi et al in view of Pidutti et al discloses the invention as described above in this office action, but fails to disclose a pre driver

including a fifth transistor coupled between the input and H-switch first transistor; and a sixth transistor as claimed.

Schuelke et al however discloses a pre driver including a fifth and a sixth transistor as claimed (see fig.2 elements Q5 and Q6 and disclosure thereof).

It would have been obvious to one of ordinary skill in the art at the time this invention was made to modify Nayebi et al in view of Pidutti et al with the above teaching from Schuelke et al ~~inoreder~~ in order to provide a write driver having a pre driver to enable desired signal amplification and hence to improve the signal to noise ratio as taught by Schuelke et al.

Claims 11-12 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nayebi et al in view of Pidutti et al as applied to claim 1, 4-6 and 13 above, and further in view of Leighton et al (6,121,800).

With regards to claims 11-12 and 18, Nayebi et al in view of Pidutti et al discloses the invention as described above in this office action, but fails to further specify that the write driver comprises a first resistor coupled between the first node and the second transistor and a second resistor couple between the second node and the forth transistor and the sum of the resistance are matched to the impedance of the write head.

However such is disclosed by Leighton et al (see fig. 1 elements R1 and R2 and disclosure thereof).

It would have been obvious to one of ordinary skill in the art at the time this invention was made to modify Nayebi et al in view of Pidutti et al with the above teaching from Leighton et al ~~inoreder~~ in order to provide a write driver having impedance matching circuit capability in order to provide an resistance value matched to the

impedance of the write head to minimize the ringing and improve the quality of the signal thereof as taught by Leighton et al.

Reasons For Allowance

Claims 3, 7-10, 19, 21 and 23 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With regards to claims 3, 19 and 23, prior art of record discloses the pre driver to drive the H-switch but fails to disclose that the transient current of the pre-driver drive the boosting transistors as recited in claims 3,9 and 23.

Claims 7-10 differs from the prior art of record by specifically reciting that the first and second PMOS transistors of the first boosting transistor set are coupled in parallel.

Claim 21 differs from the prior art of record by specifically reciting in the write driver, the H-switch is disposed between an upper and lower voltage rail, the first transistor has a base, and wherein the second boosting transistor is adapted to pull the first transistor base toward upper voltage rail and the first node toward the lower voltage rail.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Varsha A Kapadia whose telephone number is (703) 305-4198. The examiner can normally be reached on Mon Tue and Thurs. from 6:30 AM to 2:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sihn Tran can be reached on (703) 305- 4040. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VK

Primary Examiner
Wong
for SPE S. Tran